SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin-film semiconductor having crystallinity and also to a method of fabricating such a thin-film semiconductor. Furthermore, the invention relates to a semiconductor device utilizing such a thin-film semiconductor. In addition, the invention relates to a method of fabricating this semiconductor device.

2. Description of the Related Art

Techniques for forming a crystalline silicon film on a glass substrate or quartz substrate and fabricating thin-film transistors (TFTs) from this silicon film are known.

These TFTs are known as high-temperature polysilicon TFTs or low-temperature polysilicon TFTs.

High-temperature polysilicon TFT fabrication is a technique utilizing a heat treatment conducted at relatively high-temperatures such as 800°C, 900°C, and more, in fabricating crystalline silicon films. It can be said that this technique has derived from IC fabrication processes making use of single-crystal silicon wafers.

Of course, quartz substrates withstanding the above-described heating temperatures are used as substrates on which high-temperature polysilicon TFTs are formed.

On the other hand, low-temperature polysilicon TFTs are fabricated on cheaper glass substrates which are, of course, inferior in heat resistance to quartz substrates.

When a crystalline silicon film forming low-temperature polysilicon TFTs is fabricated, a heat treatment at a temperature lower than 600°C is used so that the glass

1

substrate can stand up to it, or laser annealing technique which hardly thermally damages the glass substrate is exploited.

High-temperature polysilicon TFT fabrication technology is characterized in that it can integrate TFTs having uniform characteristics on a substrate at a high density.

On the other hand, low-temperature polysilicon TFTs can make use of glass substrates which are cheap and can easily provide large areas.

It is to be noted that with the current technology, high-temperature polysilicon TFTs do not differ greatly from low-temperature polysilicon TFTs in characteristics. The slight differences between them are that high-temperature polysilicon TFTs are superior in production yield and uniformity of characteristics across the substrate while low-temperature polysilicon TFTs are superior in productivity and production cost.

With respect to the characteristics, both kinds of TFTs show mobilities of approximately 50 to 100 cm^2/ V s and S values of about 200 to 400 mV/dec (V_D = 1 V).

These characteristics mean that these TFTs can operate at speeds about two orders of magnitude higher than those of TFTs using amorphous silicon. However, the characteristics of the high-temperature polysilicon TFTs are much inferior to those of MOS transistors using single-crystal silicon wafers. Generally, the S values of MOS transistors employing single-crystal silicon wafers are on the order of 60 to 70 mV/dec. Furthermore, their operating frequencies are 1-2 orders of magnitude higher than those of high- and low-temperature polysilicon TFTs.

At present, TFTs are used to integrate the active matrix circuit of an active matrix liquid crystal display and its

2

peripheral driver circuit on the same substrate. That is, the active matrix circuit and peripheral driver circuit are fabricated from TFTs on the same substrate.

In this configuration, the source driver circuit of the peripheral driver circuit is required to operate considerably above 10 MHz. Today, however, with respect to a circuit composed of high- and low-temperature polysilicon TFTs, a margin of only several megahertz is given to the operating speed.

Accordingly, it is customary to multiplex the operation, so that a matrix-driven liquid crystal display is fabricated. However, this method has the disadvantage that stripes appear on the viewing screen due to subtle deviations of timing of multiplexing.

A conceivable forthcoming technique is to integrate oscillator circuits, D/A converters, A/D converters, and digital circuits for performing various kinds of image processing on the same substrate, in addition to the peripheral driver circuit including a shift register circuit and a buffer circuit.

However, it is necessary that the aforementioned oscillator circuits, D/A converters, A/D converters, and digital circuits for performing various kinds of image processing operate at higher frequencies than the peripheral driver circuit.

Therefore, it is substantially impossible to fabricate these circuits from the high- and low-temperature polysilicon TFTs obtained by the current techniques.

It is to be noted that an integrated circuit which consists of MOS transistors using a single-crystal silicon wafer and can be operated above 100 MHz has been put into practical use.

3

SUMMARY OF THE INVENTION

The invention disclosed herein is intended to provide TFTs capable of building a circuit which can be operated at the above-described high speeds (generally, more than tens of megahertz).

It is another object of the invention to provide TFTs having characteristics comparable to those of MOS transistors fabricated, using a single-crystal silicon wafer. It is a further object of the invention to provide means for fabricating these TFTs. It is a yet other object of the invention to provide a semiconductor device to which requisite functions are imparted by TFTs having such excellent characteristics.

A semiconductor device according to the present invention comprises a plurality of TFTs formed on a substrate having an insulating surface. The active layer of the TFTs is formed by a crystalline silicon film. This crystalline silicon film is formed by making use of crystals grown radially from a multiplicity of points.

This structure is obtained where the TFTs are fabricated, using the crystalline silicon film grown into morphologies shown in Figs. 3 and 6.

Examples of substrates having insulating surfaces include glass substrates (which are required to withstand the process temperature), quartz substrates, and semiconductor substrates having insulating films formed thereon.

The above-described crystalline silicon film consisting of crystals grown radially from a multiplicity of points can be obtained by performing crystallization step, formation of a thermal oxide film, and removal of the thermal oxide film. The aforementioned crystallization is carried out by a heat

4

treatment, using a metallic element (typified by nickel as described later) that promotes crystallization of silicon. The thermal oxide film described above is formed in an oxidizing ambient containing a halogen element.

Another semiconductor device according to the invention also comprises a plurality of TFTs formed on a substrate having an insulating surface. The active layer of the TFTs is formed by a crystalline silicon film. This crystalline silicon film is composed of a multiplicity of elongated crystalline structures grown in a certain direction. The widths of these crystalline structures range from dimensions comparable to the film thickness to 2000 Å. The certain direction differs among the individual TFTs.

More specifically, where a number of TFTs are manufactured, using the crystalline silicon film grown into the crystal morphologies shown in Figs. 3 and 6, the crystal growth direction (the direction of anisotropy of the elongated structures) in the active layer forming the TFTs differs among the individual TFTs.

Of course, some TFTs have active layers having the same crystal growth direction but most of the TFTs adopt the above-described structure.

For example, if an active matrix circuit is made of a crystalline silicon film consisting of crystals grown into a morphology as shown in Fig. 3, numerous TFTs arranged in hundreds of devices x hundreds of devices achieve the above-described structure.

The crystalline silicon film used in the present invention disclosed herein consists of crystals which are continuous with each other in a certain direction, as shown in Fig. 8. These successive elongated crystal structures have widths ranging from dimensions comparable to the film

5

thickness to about 2000 Å. These numerous crystal structures form regions which extend substantially parallel on opposite sides of grain boundaries.

Macroscopically, these crystal structures extend radially as shown in Figs. 7 and 6.

A method according to the present invention comprises the steps of: forming an amorphous silicon film on an insulating surface; crystallizing the amorphous silicon film by the action of a metallic element that promotes crystallization of silicon to obtain a crystalline silicon film; performing thermal processing at 800-1100°C in an oxidizing ambient containing a halogen element to form a first thermal oxide film on a surface of the crystalline silicon film; removing the first thermal oxide film; and forming a second thermal oxide film on the surface of the crystalline silicon film, whereby obtaining a final crystalline silicon film consisting of crystals grown radially from a multiplicity of points.

In the above-described method, in order to improve the quality of the final crystalline silicon film, it is important to make the total thickness of the first and second thermal oxide films greater than the thickness of the final crystalline silicon film.

This is because the formed thermal oxide films drastically improve the quality of the crystalline silicon film.

Nickel is used quite advantageously as the metallic element for promoting crystallization of silicon in terms of reproducibility and effects. Generally, one or more elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au can be used as this metallic element.

Where nickel element is employed, the concentration of nickel finally remaining in the silicon film is approximately 1×10^{14} to 5×10^{18} atoms/cm^3. If the gettering conditions for the thermal oxide films are optimized, the upper limit of this concentration can be reduced to about 5×10^{17} atoms/cm^3. The concentration can be measured by SIMS (secondary ion mass spectroscopy).

Generally, the lower limit of the nickel concentration is approximately 1×10^{16} atoms/cm^3. That is, this amount of nickel is left behind because it is normally difficult to remove the effects of nickel adhering to the substrate or equipment if the cost is also taken into account. However, the concentration of the residues can be reduced further by cleaning the equipment to a higher level or improving the manufacturing processes.

Accordingly, where general manufacturing processes are adopted, the concentration of the remaining nickel element is about 1×10^{16} to 5×10^{17} atoms/cm^3.

During fabrication of a thermal oxide film, the metallic element moves into the thermal oxide film and so the concentration of nickel element in the direction of thickness of the obtained crystalline silicon film has a gradient or distribution.

Generally, it is observed that the concentration of the metallic element in the crystalline silicon film tends to increase toward the interface at which the thermal oxide film is formed. Furthermore, it is observed that depending on the conditions, the concentration of the metallic element tends to increase toward the substrate or buffer layer, i.e., toward the interface on the back side.

Where a halogen element is added to the ambient when a thermal oxide film is formed, this halogen element shows a

concentration distribution similar to that of the metallic element. That is, the concentration distribution is such that the concentration increases toward the front surface and/or rear surface of the crystalline silicon film.

The thickness of the final crystalline silicon film according to the present invention is preferably set to 100 to 750 Å, more preferably 150 to 450 Å. By selecting the film thickness in this way, the crystalline structure shown in Figs. 6-8 can be obtained more clearly and with improved reproducibility.

It is necessary that the thickness of the final crystalline silicon film be determined by taking account of the fact that the film thickness is reduced by the deposition of the thermal oxide film.

The crystalline silicon film described herein can be obtained by adopting the manufacturing steps described above. Furthermore, MOS TFTs utilizing the special features of the crystalline structure can be obtained.

Examples of the method of introducing the metallic element include application of a solution containing this metallic element, a method using a CVD process, methods relying on sputtering or deposition, a plasma processing method using an electrode containing this metal, and a method making use of gas adsorption.

A method of introducing a halogen element can use a means for adding HCl, HF, HBr, Cl_2, F_2, Br_2, or CF_4 to an oxidizing ambient such as oxygen ambient.

Furthermore, when the thermal oxide film is fabricated, if hydrogen gas is also introduced into the ambient to make use of the action of wet oxidation, then desirable results arise.

The temperature at which the thermal oxide film is grown

is quite important. If one attempts to obtain a TFT which can be operated by itself at tens of megahertz or more and shows an S value of less than 100 mV/dec as described later, then it is necessary to set the heating temperature used during the formation of the thermal oxide film above 800°C, more preferably 900°C or above.

The upper limit of this heating temperature should be set to about 1100°C which is the maximum processing temperature of quartz substrates.

The present invention lies in a technique for crystallizing an amorphous silicon film by means of heating to obtain a crystalline silicon film. This technique is characterized in that thermal processing is performed while holding nickel element in contact with the surface of the amorphous silicon film, thus giving rise to the crystalline silicon film. A thermal oxide film is formed on the surface of this crystalline silicon film by performing thermal processing at 800-1100°C in an oxidizing ambient containing a halogenic element.

Thus, a crystalline silicon film grown into the peculiar crystalline state as shown in Figs. 6-8 can be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(A)-1(D) are views illustrating a process sequence for fabricating a TFT;

Figs. 2(A)-2(E) are views illustrating a process sequence for fabricating a TFT;

Fig. 3 is a diagram conceptually illustrating the state of grown crystals;

Figs. 4(A)-4(D) are views illustrating a process sequence for fabricating a TFT;

Figs. 5(A)-5(E) are views illustrating a process sequence for fabricating a TFT;

9

Fig. 6 is an electron micrograph of a thin silicon film;

Fig. 7 is an electron micrograph of another thin silicon film;

Fig. 8 is an electron micrograph of a further thin silicon film; and

Figs. 9(A)-9(F) are views schematically showing semiconductor devices according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

EMBODIMENT 1

The present embodiment relates to a method of obtaining a crystalline silicon film grown into a peculiar morphology as shown in Fig. 6, by introducing a metallic element for promoting crystallization of silicon into the whole surface of an amorphous silicon film.

The process sequence of the present invention is shown in Figs. 1(A)-1(D). First, a silicon oxide film is formed as a buffer layer 202 on a quartz substrate 201 to a thickness of 3000 Å. If the surface of this quartz substrate has excellent flatness and is cleaned sufficiently, then this buffer layer 202 may be dispensed with.

At present, it is desired to use the quartz substrate. However, the material of the substrate is not limited to quartz as long as the substrate is capable of withstanding the heating temperature during the thermal processing. For instance, a semiconductor substrate having an oxide film deposited thereon may also be used.

Then, an amorphous silicon film 203 acting as a starting film for a crystalline silicon film is formed to a thickness of 500 Å by LPCVD.

Thereafter, nickel acetate solution containing 10 ppm (weight-converted value) of nickel element is applied.

10

Then, a spin-drying process is carried out, using a spinner (not shown), to remove a surplus of solution.

In this way, nickel elements are present as shown by the dotted line 204 in Fig. 1(A) to obtain a state shown in Fig.1(A).

Among methods of introducing nickel, the above-described method using the solution is excellent in controllability of the introduced amount and reproducibility. However, a metallic element (typified by nickel) for promoting crystallization of silicon may be introduced by a method using a CVD process, sputtering, plasma processing, gas adsorption, or other method.

Then, thermal processing is conducted at 600°C for 8 hours in a nitrogen ambient which contains 3% hydrogen but contains a minimum amount of oxygen. As a result of this thermal processing, crystallization proceeds. Consequently, a crystalline silicon film 205 shown in Fig. 1(B) is derived.

This thermal processing for crystal growth can be carried out at 450-1100°C. The upper limit of this temperature range is restricted by the heat resistance of the substrate. If some lateral growth distance should be secured, it is desired to set the heating temperature used in the heating processing to 600°C or above. However, elevating the temperature further does not increase the crystal growth distance and crystallinity so much.

After the crystallization relying on this heating, laser light irradiation may be performed. That is, the crystallization may be promoted further by laser light irradiation. This irradiation acts to disperse nickel element clusters existing in the film. This will facilitate removing the nickel element later. Even if laser light

11

irradiation is effected at this stage, lateral growth will no longer proceed.

The laser light can be emitted by an excimer laser having a wavelength lying in the UV range. For example, a KrF excimer laser (producing a wavelength of 248 nm) or XeCl excimer laser (producing a wavelength of 308 nm) can be exploited.

After the end of the thermal processing for the crystallization, a heat treatment is done at 950°C in an oxygen ambient containing 3% by volume of HCl. During this step, a thermal oxide film 209 is formed to a thickness of 200 Å on the surface of the crystalline silicon film 205 (Fig. 1(C)).

As a result of the formation of this thermal oxide film, the thickness of the crystalline silicon film 208 decreases by about 100 Å. That is, the thickness of the silicon film assumes a value of approximately 400 Å.

During this step, as the thermal oxide film is formed, silicon element having unstable bonds in the film is used for the formation of the thermal oxide film. Defects in the film decrease, so that better crystallinity can be obtained.

At the same time, nickel element is gettered out of the film because of the formation of the thermal oxide film and by the action of chlorine.

Of course, a relatively high dose of nickel elements gets incorporated into the thermal oxide film 209 formed by this step. The relative concentration of nickel element within the silicon film 208 decreases.

After the formation of the thermal oxide film 209, it is removed. In this way, the crystalline silicon film 208 less doped with nickel element is obtained (Fig. 1(D)).

In the crystalline silicon film obtained in this manner,

12

crystals are grown radially from many local regions (many points) as shown in Fig. 6, which is a photograph of an enlarged image obtained by an optical microscope.

Fig. 7 is an enlargement of a part of Fig. 6, and is a photograph take by a TEM (transmission electron microscope).

In this crystalline structure, grain boundaries extend in the direction in which crystals are grown radially. Also, crystalline structures are continuous with each other in this direction. It is confirmed that the continuity of crystal lattices is substantially maintained in this direction.

Fig. 8 is an enlargement of a part of Fig. 7, and is a photograph of an image observed with a TEM. Fig. 3 pictorially shows the state of crystals grown over the whole film.

In this obtained crystalline silicon film, the crystalline structures extend in one direction which is coincident with the crystal growth direction, as shown in Figs. 6 and 7. That is, a plurality of crystalline columns are arranged parallel on opposite sides of grain boundaries extending in one direction.

These successive crystalline columns have widths ranging from dimensions comparable to the film thickness to approximately 2000 Å. Microscopically, they form regions extending substantially parallel on opposite sides of grain boundaries extending in a certain direction that is substantially coincident with the direction in which the above-described crystalline columns are continuous with each other.

After the thermal oxide film 209 is removed and the crystalline silicon film 208 as shown in Fig. 1(D) is obtained, a patterning operation is carried out to create a

13

pattern 302 consisting of laterally grown regions. These islands of region 302 will become an active layer for a TFT later.

Then, as shown in Fig. 2(A), after the formation of the pattern 302, a silicon oxide film 304 is formed to a thickness of 1000 Å by plasma CVD. This silicon oxide film 304 will act as a gate-insulating film later.

After forming the silicon oxide film 304, a heat treatment is performed at 950°C in an oxygen ambient containing 3% HCl to form a thermal oxide film 303 having a thickness of 300 Å. This thermal oxide film is formed on the surface of the pattern 302 becoming the active layer, as shown in Fig. 2(A).

As a result of the thermal oxide film 211, the thickness of the pattern 302 becoming the active layer reaches 250 Å.

If a TFT of higher performance should be obtained, it is desired that the thermal oxide film 303 be thicker than the crystalline silicon film forming the active layer.

In general, it is important that the total thickness of the thermal oxide films 209 and 303 be greater than the thickness of the finally obtained active layer.

This thermal oxide film 211 forms parts of the gate-insulating film. In this way, a state shown in Fig. 2(A) is obtained.

Then, an aluminum film forming gate electrodes is formed to a thickness of 4000 Å by sputtering. This aluminum film contains 0.2% by weight of scandium.

The incorporation of the scandium in the aluminum film is intended to suppress generation of hillocks and whiskers at later processing steps. The hillocks and whiskers are needle-like or prickle-like protrusions due to overgrowth of aluminum during heating.

After the formation of the aluminum film, a dense anodic oxide film (not shown) is formed. For this purpose, an anodization process is carried out, using ethylene glycol solution containing 3% tartaric acid. The aluminum film is used as an anode, and a cathode of platinum is also employed. In this step, the dense anodic oxide film is formed to a thickness of 100 Å on the aluminum film.

This anodic oxide film (not shown) serves to improve the adhesion to a resist mask formed later.

The thickness of this anodic oxide film can be controlled by the voltage applied during the anodization.

Then, the resist mask, indicated by 306, is formed. The aluminum film is patterned into stripes 305, utilizing this resist mask. As a result, a state shown in Fig. 2(B) is obtained.

Anodization is again effected. During this step, 3% aqueous solution of oxalic acid is used as an electrolytic solution. Within this electrolytic solution, the anodization is carried out, using the aluminum pattern 305 as an anode. Consequently, a porous anodic oxide film 308 is formed (Fig. 2(C)).

In this step, the anodic oxide film 308 is formed selectively on the side surface of the aluminum pattern because the resist mask 306 adhering well exists thereon.

This anodic oxide film can be grown to a thickness of several micrometers. In this embodiment, the film thickness is set to 6000 Å. The growth distance can be controlled by the anodization time.

Then, the resist mask 306 is removed. Subsequently, another dense anodic oxide film is formed. In particular, anodization is again performed, using an electrolytic solution consisting of the aforementioned ethylene glycol

15

solution containing 3% tartaric acid.

During this step, the electrolytic solution intrudes into the porous anodic oxide film 308 and so a dense anodic oxide film 309 is formed.

The thickness of this dense anodic oxide film 309 is set to 1000 Å. This film thickness is controlled by the applied voltage.

Then, the exposed silicon oxide film 304 is etched away. At the same time, the thermal oxide film 303 is etched by dry etching techniques.

The remaining, CVD-grown silicon oxide film is indicated by 310. A thermal oxide film of the similar shape is left behind under the left silicon oxide film.

In this way, a state shown in Fig. 2(C) is obtained. The porous anodic oxide film 308 is removed, using mixed acid of acetic, nitric, and phosphoric acids. In this manner, a state shown in Fig. 2(D) results.

After obtaining the state shown in Fig. 2(D), dopant ions are implanted. In this embodiment, phosphorus (P) ions are introduced by plasma doping.

During this step, heavily doped regions 311, 315 and lightly doped regions 312, 314 are formed, because the remaining silicon oxide film 310 acts as a semi-transparent mask (a semi-blocking mask) and block some of the implanted ions.

Laser light or other intense light from a lamp is irradiated to activate the dopant ion-implanted regions. In this way, the source region 311, a channel-forming region 313, the drain region 315, and lightly doped regions 312, 314 are formed by self-aligned technology.

The region 314 is a lightly doped drain (LDD) region (Fig. 2(D)).

16

Where the thickness of the dense anodic oxide film 309 is increased to 2000 Å or more, this great thickness permits formation of an offset gate region outside the channel-forming region 313.

Also in the present invention, an offset gate region is formed but its dimensions are small. Hence, the contribution of the offset gate region is small and not shown for simplicity.

When the dense anodic oxide film is made as thick as 2000 Å or more, it is necessary to apply a voltage of more than 200 V. Hence, care must be taken to secure sufficient reproducibility and safety.

After obtaining the state shown in Fig. 2(D), a silicon nitride film 300 is formed as an interlayer dielectric film by plasma CVD. Then, a polyimide resin film 316 is formed by spin coating.

Thereafter, a contact hole is formed. A source electrode 317 and a drain electrode 318 are formed. In this way, a TFT shown in Fig. 2(E) is completed.

The TFT of the present embodiment shows unparalleled characteristics.

For example, a high-performance NTFT (N-channel TFT) having a mobility of 200 to 300 $cm^2/$ V s and an S value of 75 to 90 mV/dec (V_D = 1 V) is obtained. Furthermore, a high-performance PTFT (P-channel TFT) having a mobility of 120 to 180 $cm^2/$ V s and an S value of 75 to 100 mV/dec (V_D = 1 V) is derived.

Especially, these S values are less than half of those of the conventional high-temperature and low-temperature polysilicon TFTs. That is, these are surprisingly excellent values.

Using these TFTs, an operational amplifier, memory

circuits, various kinds of arithmetic circuits and amplifiers can be formed on a quartz substrate.

EMBODIMENT 2

The present embodiment shows processing steps for fabricating the active matrix circuit portion of an active matrix liquid crystal display.

The process sequence of the present embodiment is schematically shown in Figs. 4(A)-4(D). A crystalline silicon film and a liquid crystal display are fabricated by the fabrication steps described in Embodiment 1. A state shown in Fig. 2(D) (Fig. 4(A)) is obtained by the fabrication steps shown in Figs. 1(A)-1(D) and 2(A)-2(D).

After obtaining the state shown in Fig. 4(A), a silicon nitride film 401 is formed as a first interlayer dielectric film to a thickness of 2000 Å by plasma CVD. Then, a polyimide resin film 402 is spincoated. Thus, a state shown in Fig. 4(B) is obtained. Polyamide and polyimideamide can be used as resinous materials, as well as polyimide.

Then, contact holes extending to the source region 311 and to the drain region 315 are formed. A source electrode 403 and a drain electrode 403 are created. These electrodes are fabricated from a Ti-Al-Ti lamination film. The source electrode 403 is formed so as to extend from a source line (Fig. 4(C)).

Portions of the drain electrode 403 are employed as electrodes for forming an auxiliary capacitor.

After forming the source and drain electrodes, a polyimide resin film 404 is formed as a second interlayer dielectric film. Thus, a state shown in Fig. 4(C) is derived.

Then, a window is formed in the resinous interlayer

18

dielectric film 404. A black matrix (BM) 405 is fabricated from a lamination film of titanium and aluminum. Inherently, this black matrix 405 acts as a light-shielding film. Besides, this black matrix serves as electrodes forming auxiliary capacitors.

After forming the black matrix 405, a polyimide resin film 406 is formed as a third interlayer dielectric film. A contact hole that permits access to the drain electrode 403 is formed. A pixel electrode pattern 407 is formed from ITO.

The pattern of the black matrix 405 overlaps the pattern of the pixel electrode 407 via the polyimide resin film 406, thus forming the auxiliary capacitors.

EMBODIMENT 3

The present embodiment is similar to Embodiment 1 except that contacts are formed either on gate electrodes or on gate interconnects extending from the gate electrodes by a novel method.

In Embodiment 1, the side and top surfaces of the gate electrodes are coated with the dense anodic oxide film.

Where the electrodes are fabricated from aluminum, this structure is very effective in suppressing hillocks and shorts between conductive interconnects.

However, the densification of the film makes it relatively difficult to form contacts.

The present embodiment relates to a structure for solving this problem. The process sequence of the present embodiment is shown in Figs. 5(A)-5(E). It is to be noted that like components, including details of fabrication conditions, are indicated by like reference numerals in various figures.

First, as shown in Fig. 5(A), an active layer pattern 210 is formed from a crystalline silicon film. A lamination

layer consisting of a thermal oxide film 211 and a CVD-grown oxide film 304 is formed thereon.

In this embodiment, the CVD-grown oxide film is first formed, followed by formation of the thermal oxide film.

After obtaining the state shown in Fig. 5(A), an aluminum film is formed, and a silicon nitride film is formed to a thickness of 500 Å. The laminate is patterned, using a resist mask 306. As a result, an aluminum pattern 305 and an overlying silicon nitride film pattern 501 are formed (Fig. 5(B)).

After obtaining the state shown in Fig. 5(B), a porous anodic oxide film 308 is formed while leaving the resist mask 306 behind. A denser anodic oxide film 309 is formed.

These anodic oxide films are formed selectively only on the side surfaces of the aluminum pattern 307 becoming gate electrodes, because the top surface of the aluminum pattern is capped with the silicon nitride film 501.

After the formation of the anodic oxide film, the resist mask 306 is removed. The exposed silicon oxide film 304 is also removed. The thermal oxide film 211 is partially removed.

In this way, a state shown in Fig. 5(C) is obtained. Then, the resist mask 306 is removed, and the porous anodic oxide film 308 is removed.

Subsequently, the silicon nitride film 501 is removed. This results in a state shown in Fig. 5(D). Under this condition, a dopant that imparts a conductivity type is implanted by plasma doping.

As a result, a source region 311, lightly doped regions 312, 314, a channel region 313, and a drain region 315 are formed by self-aligned technology.

After the dopant doping, laser light irradiation is

performed to anneal out the damage caused by the doping and to active the introduced dopant.

In this way, a state shown in Fig. 5(D) arises. Then, an interlayer dielectric film 502 is formed. A contact hole is formed. A source electrode 317, an electrode 503 extending from the gate, and a drain electrode 318 are formed. Thus, a state shown in Fig. 5(E) is obtained.

During this step, the formation of the contact hole extending to the gate electrode 307 can be performed relatively easily because no anodic oxide film resides on top of the gate electrode.

Source/drain electrodes and gate electrode are shown to be formed on the same cross section but, in practice, the electrode 503 is formed on a part of the gate electrode 307 extending from the gate electrode 307.

EMBODIMENT 4

The present embodiment is an improvement over the configuration of Embodiment 3. In the present embodiment, a titanium film is grown on the aluminum film forming the gate electrode. A silicon nitride film is formed on the titanium film.

In particular, in a configuration shown in Fig. 5(B), the film 501 is made of a lamination film of titanium and silicon nitride. This can suppress generation of hillocks on the top surface of the aluminum electrode in later processing steps.

EMBODIMENT 5

The present embodiment is similar to Embodiment 1 except that the substrate is made of glass.

In the present embodiment, the substrate is made of Corning 1737 glass having a strain point of 667°C. A heat treatment is made at 600°C for 4 hours for crystallization.

21

A heat treatment for formation of a thermal oxide film is carried out at 640°C in an oxygen ambient containing 3% by volume of HCl. In this case, the thickness of the thermal oxide film formed reaches about 30 Å if the processing time is 2 hours. The resulting effect is smaller compared with the case where a heat treatment at 950°C is added as in Embodiment 1.

EMBODIMENT 6

The present embodiment is similar to Embodiment 1 except that the ambient in which the thermal oxide film is formed does not contain HCl. In this case, the gettering effect of nickel is smaller than in the case where the ambient contains HCl.

EMBODIMENT 7

The present embodiment is similar to Embodiment 1 except that laser light irradiation is carried out after the formation of the thermal oxide film. This can promote the crystallization further.

EMBODIMENT 8

The present embodiment shows examples of semiconductor device making use of TFTs. These various examples of semiconductor device are shown in Figs. 9(A)-9(F).

Referring to Fig. 9(A), there is shown a portable intelligent terminal whose body is indicated by 2001. The body comprises an active matrix liquid crystal display 2005 including a memory. Required information can be read from the internal memory and displayed on the display 2005. Furthermore, information accessed through a telephone line can be displayed on the display 2005.

It can be considered that the display device is an active matrix electroluminescent device. Various information-processing circuits and storage circuits are

22

fabricated as an integrated circuit 2006, using TFTs, on the same substrate as the active matrix circuit forming the display device.

The body 2001 is equipped with a camera portion 2002. Required image information can be picked up by operating an operation switch 2004. The image picked up by the camera portion 2002 is accepted into the instrument through an image-receiving portion 2003.

Referring next to Fig. 9(B), there is shown a head mounted display whose body is indicated by 2101. A user puts on this body 2101. This display unit has two active matrix liquid crystal displays 2102 which act to display images in a location several centimeters away from the user's eyes. This instrument permits virtual reality visualization.

Referring next to Fig. 9(C), there is shown a car navigational system. This system acts to measure positions, using signals from an artificial satellite, the signals being received by an antenna 2204. The measured positions are displayed on an active matrix liquid crystal display 2202. The displayed information is selected with an operation switch 2203.

Instead of the liquid crystal display, an active matrix electroluminescent display can be utilized.

An example of mobile telephone is shown in Fig. 9(D). The body of this apparatus is indicated by 2301 and equipped with an antenna 2306. The apparatus has a speech input portion 2303 and a speech output portion 2302.

When the user telephones, operation switches 2305 are operated. Various kinds of image information are displayed on a display unit 2304. To make the display unit portable, an active matrix liquid crystal display or active matrix

electroluminescent display is employed.

Shown in Fig. 9(E) is a portable video camera whose body is indicated by 2401. This apparatus has an image-receiving portion 2406 for picking up an image. This image is stored in a magnetic tape loaded in the body 2401.

An integrated circuit 2407 performs various kinds of digital processing on the image. This integrated circuit 2407 may be a combination of conventional ICs chips or a combination of TFTs disclosed herein. Furthermore, these two types of devices may be combined.

The image received by the image-receiving portion 2406 or stored in the internal magnetic tape is displayed on the active matrix liquid crystal display 2402. The apparatus is controlled with operation switches 2404 and powered by a battery 2405.

Shown in Fig. 9(F) is a projection display system whose body is indicated by 2501. An image projected by the body 2501 is displayed on a screen.

The body 2501 comprises a light source 2502, an active matrix liquid crystal display 2503 for optically modulating the light from the light source and forming an image, and optics 2504 for projecting the image.

Excluding the apparatus shown in Fig. 9(B), the liquid crystal display can be either transmission type or reflection type.

Where a 9-stage ring oscillator is built by combining PTFTs and NTFTs obtained by making use of the invention disclosed herein, oscillations above 400 MHz are possible.

Generally, an actual circuit is designed to operate at about 10% of the oscillation frequency of the ring oscillator. Where this fact is taken into account, it can be said that a circuit operating at frequencies of about 40

24

MHz can be fabricated from the above-described TFTs.

In this way, thin-film transistors (TFTs) capable of forming a circuit which is required to operate at high speeds (generally, tens of megahertz or above) can be obtained by exploiting the invention disclosed herein.

Accordingly, for example, without operating the peripheral driver circuit of an active matrix liquid crystal display by a multiplexing scheme, the peripheral driver circuit can be integrated with the active matrix circuit on the same substrate.

With respect to S values, characteristics comparable to those of MOS transistors fabricated, using a single-crystal silicon wafer of less than 100 mV/dec, can be obtained.

A circuit which is required to exhibit various high-speed operations can be fabricated as an integrated circuit from TFTs on the same substrate by utilizing the invention disclosed herein. Furthermore, a method of fabricating this circuit is provided.